T H E E L E C T R O N

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NATIONAL ELECTRONICS WEEK

One of the UK's major exhibitions for electronics professionals in 2014 was National Electronics Week, a biennial event which this year was held The National Exhibition Centre in Birmingham from 8th. to 10th. April.

Over 100 exhibitors were featured in four categories as follows:

- Design and Test
- Components and Power
- Embedded and Software
- Production and EMS

This was supported with a comprehensive seminar programme consisting of around 30 different presentations on a diverse range of subjects such as 'CE Marking your Electrical and Electronic Equipment', 'Reducing Time to Market with Advanced Thermal Modelling Techniques', 'Improving Signal Fidelity with FPGA Signal Averaging on PXI Module', 'Improving Electronic Product Quality through Measurement Data Intelligence, 'Verification Techniques for better Code and higher Productivity', and 'a3Di: A new Concept in Loaded PCB Inspection'.

Some of the latest developments promoted at the exhibition are featured below.

INTRODUCING THE AdaCore UNIVERSITY

Today's computer programming languages such as Python, Java, C++, C# and Visual Basic offer functionality that can meet the needs of any programmer. With them it is possible to write code quickly and in some cases they can even allow compilers to deduce the developer's probable intent. They do, however, have their weaknesses, particularly when it comes to working within the domain of high-integrity systems.

In applications where failure could potentially jeopardise lives or critical assets the programming languages used must be able to support the high standard of software engineering that is necessary in order to maintain the integrity of the system.

The concept of verification, that is the practice of showing that the system behaves and performs as intended, is of paramount importance in such environments. It is achieved usually by a combination of review, testing, static analysis, and formal proof techniques, but the increasing reliance on software combined with the increasing complexity of systems has made verification increasingly difficult to the point that technologies and practices that may have been acceptable a decade ago now are not.

This situation has resulted in increased attention being given to the Ada language which, ever since its inception in the 1980s, has aimed to meet the requirements of high-integrity systems. In Ada 2012 new features for contract-based programming that are valuable to any project where verification is part of the engineering lifecycle, have therefore been introduced. Ada development environments are also available on a wide range of platforms and are being used for the most demanding applications.

In order to make it easier for developers to quickly come to speed in Ada, a free web-based educational resource centre known as The AdaCore University, has been launched by AdaCore. This site contains pre-recorded courses and other learning materials and provides access to AdaCore's GNAT Ada toolset for writing and running example programs. With this students at all levels can begin writing programs quickly and can proceed at their own pace. There are also flexible controls for navigating through the lessons.

The courses educate through examples that allow students to see, understand and experiment with most features of the Ada programming language. Each course includes one or more interactive quizzes, with detailed explanations of the solutions and explanation of Ada's technical concepts, with insight into the rationale and usage of particular features being given.

The initial curriculum includes two courses, presented by AdaCore University project leader Quentin Ochem as follows:

- Ada 001 (Overview) module presenting an overall picture of the language and demonstrating how to build and run programs.

- Ada 002 (Basic Concepts) module with lessons on Basic Types, Statements, Arrays, Records, Subprograms and Packages.

These courses are complemented with a set of lab exercises that reinforce the concepts of Ada 2012 such that students will learn about the new features such as contract-based programming, and SPARK 2014 – a new version of the Ada-based SPARK programming language for high-integrity software.

In addition to the above a free guidebook called 'Ada for the C++ or Java Developer' by Quentin Ochem explains the Ada language using analogies to the C++ and Java languages that many programmers will be familiar with prior to learning Ada.

Further information is available from AdaCore, 46 rue d'Amsterdam, 75009 Paris, France. www.adacore.com

SME FUNDING FOR CE COMPLIANCE

The CE Marking Association has announced compliance assistance funding for small and medium sized enterprises in the UK, offering funding of up to 50 per cent for certain types of projects to help them through the CE Marking process.

The projects covered include:

- Testing and assessments
- EMC design advice
- Conducting of risk assessments
- Electrical safety testing
- In-company consultancy
- Definition and interpretation of standards
- International compliance guidance
- Technical (construction) file compilation
- Knowledge transfer workshops and training

Applicants must typically be a UK SME manufacturing company with fewer than 250 employees and meet certain other basic eligibility criteria.

Further information is available on 01527 595 066.

THE SMART EMBEDDED MANAGEMENT AGENT

Today's embedded systems need to provide both optimal performance and low power consumption. This can be difficult to accomplish, however, without adequate control and system management tools to detect potential problems before they become serious. Similarly, systems have to be stable and reliable, particularly when running in critical applications and severe environments that are subject to extreme shock and/or vibration and extremes of temperature.

In order to address these requirements ADLINK has developed a tool that is able to monitor and collect system performance status information from the hardware in a

timely, flexible and precise manner. It is called the Smart Embedded Management Agent (SEMA).

One of the most important features of the SEMA is provision of the interface between the hardware and the operating system. For this the Board Management Controller (BMC) first collects all relevant information from the chipset and other sources. Then, using the System Management Bus driver, the application layer fetches the data and presents it to the user.

The board controller continuously reads out system information from the board, which can be made visible in three different ways:

(i) BIOS menu display

(ii) Display via ADLINK software application in the operating system

(iii) Data transfer to the ADLINK SEMA cloud

All three methods allow users to view and easily access board controller functions, with the SEMA cloud additionally allowing transmission of data via a 3G connection, any TCP/IP connection (such as WLAN, Ethernet or Bluetooth), or any other medium that is able to establish an Internet or M2M connection.

Compatibility with the latest Embedded Application Programming Interface (EAPI) reduces the effort required to port existing calls to SEMA to virtually zero.

The ADLINK SEMA cloud service provides an information function, alarm function and a remote control function (for the remote control of system parameters such as fan speed).

In relation to the latter ADLINK has implemented an M2M stack that allows users to set up a cloud application to control different devices. The cloud application monitors the current health status of the connected embedded systems and before a device crashes the cloud may recognise the malfunction through the SEMA functions and respond, for example by shutting down the system, before there is any serious damage.

Further information on this subject is available from LiPPERT ADLINK Technology GmbH, Hans-Thoma_Strasse 11, D-68163, Mannheim, Germany. Email: emea@adlinktech.com

COSTS SLASHED FOR SAMPLING OSCILLOSCOPES

At data rates of over 1Gb/s, circuit designers need to pay close attention to PCB design and component performance in order to ensure good signal integrity. High speed signals in densely packed designs create undesirable effects that can interfere with the correct and reliable operation of a circuit. Parts placement, trace impedance

and proper termination are critical to control crosstalk, noise jitter, ground bounce, slew rate, and reflections while maintaining proper system timing.

For such designs engineers first need to validate characteristics of the PCB backplane, interconnects and cables. Once the PCB and passive components have been checked the board can be populated, debugged and performance tested to ensure that it meets its design goals.

Digital oscilloscopes are the most popular tools for the debugging and testing of high-speed designs, offering a convenient view of circuit operating characteristics with an accurate display of wave shape, frequency, channel-to-channel timing, ringing and reflections, over- and undershoot, pulse-width and other characteristics. Automated measurements and statistics assist designers in rapidly checking the performance of critical circuit elements and advanced triggers can be used to hunt for the waveform anomalies that are frequently the root cause of design malfunction. Additional tools such as Time-Domain Reflectometry (TDR) and Time-Domain Transmissometry (TDT) may also be featured so as to extend the capabilities of the oscilloscope for the measurement of transmission line characteristics of the PCB and interconnects.

The market is well served with conventional high-performance bench-top oscilloscopes that offer 20 or 30 GHz bandwidth or higher and address multi-gigabit design challenges, but the cost can be prohibitive at $200,000 for 20GHz real-time bench-top models, and $50,000 for a 20GHz 2-channel sampling oscilloscope with built-in TDR/TDT.

In order to substantially reduce the price of this high-cost investment Pico Technology has developed a range of 20GHz USB sampling oscilloscopes that deliver the performance and functionality required by designers for characterisation of of 8Gb/s and debug of 12Gb/s designs, but at a cost of less than half of that of conventional bench-top models.

The PicoScope 9300 series comes complete with automated measurements, mask testing and a built-in pattern generator for in-line component and module testing. The range includes models with clock-data recovery to 11.3Gb/s and TDR/TDT for PCB and transmission line characterisation, plus optical measurement s to 9.5GHz.

Sequential sampling technology is used to measure fast repetitive signals without the need for expensive real-time sampling hardware. An input bandwidth of 20GHz enables acquisition of signals with rise times down to 17.5ps. Timebase resolution to 64fs allows characterisation of jitter for demanding applications.

Further information is available from Pico Technology – www.picotech.com

NEW METHOD SPEEDS UP GROUP DELAY MEASUREMENTS

Group delay measurements are especially important for ensuring the quality of sophisticated communications technologies such as those used in satellite systems. The signal deformations that result from non-constant group delay introduce intersymbol interference, which in turn increases the bit error rate at the receiver. Designs can be revised to eliminate signal distortion, but only once the distortions have been identified and measured.

Group delay indicates the time delay a signal encounters when passed through a transmission channel. It typically results from filtering and mismatch in the transmission path, which causes the signal components to undergo a frequency dependent shift.

Linear phase characteristics result in a constant group delay for all frequency components in the signal. Any deviations from linear phase cause a non-constant group delay, that is different frequency components of the signal pass the transmission channel with a different delay. This leads to distortion of the signal's envelope, and signal components of a preceding bit may interfere with the following bit.

The measurement of group delay involves measuring the signal transmit phase at various frequencies, and vector network analysers are usually used to determine group delay. This technique, however, is widely perceived to be slow and outdated, so Rohde and Schwarz have developed a new approach to supersede it.

The new approach uses a set up consisting of a signal and spectrum analyser (RandS FSW) and a vector signal generator (RandS SMBV). With this the vector signal generator generates wideband multicarrier signals in the frequency range of interest. Use of these signals makes it possible to quickly determine the group delay over a wide frequency range within one measurement instead of sweeping or stepping over the frequency range of interest. Thus, the RandS FSW and RandS SMBV in combination can measure a bandwidth of 160MHz in one shot in under 100ms. High precision measurements are possible with a measurement uncertainty of just plus or minus 300ps.

The RandS FSW-K17 software option for multicarrier group delay measurements allows the multicarrier method to be used on the RandS FSW signal and spectrum analyser. The method supports both relative and absolute group delay measurements.

The technique lends itself particularly to satellite transmission systems where, due to the complexity of transmission equipment, wideband design and efficient channel utilisation, testing requires many more measurements to determine quality. Many of these measurements require a spectrum analyser and adding group delay measurements widen the signal and spectrum analyser's range of applications in this kind of environment, for example in the design of satellite transponders or entire ground stations.

In order to ensure that the transmission equipment of a satellite can be used without decreased performance, payload tests must be carried out before the satellite is put into operation. In many cases the original signal must be measured in a different frequency band because of the frequency-converting transmission elements. The pre-configured software for the RandS FSW can handle this.

Rohde and Schwarz state:

'If the test software and testing procedure have been properly configured, only one parameter must be changed for the payload measurement – the centre frequency. The software option can create the relationship between the reference carriers of the multicarrier signal and the frequency-converted measurement signal.'

More details may be obtained from Rohde and Schwarz UK Limited, Ancells Business Park, Fleet, Hampshire GU51 2UZ. Telephone: 01252 818 888.

This and the preceding article are featured in the journal *Electronics Specifier, Volume 1, Issue 1, September 2013.*

ADVANCES IN THERMAL CONTROL FOR SOLDERING

For years soldering and desoldering technology has suffered from the disadvantage of only offering one type of heating technology, which can never fit every application efficiently. This has necessitated either multiple power source provision on the work bench or requiring operators to work with just one heating technology.

In order to eliminate these deficiencies PACE Worldwide has developed the first thermal control system that is capable of managing multiple types of heating technologies within a single power source.

The system is known as the INTELLIHEAT® Control System and utilises a combination of Tip-Heater Cartridge Technology and SensaTemp® Technology.

Tip-Heater Cartridge Technology has the advantage of advanced electronics that provide instantaneous load sensing and on-demand power to quickly reflow solder joints, regardless of the mass of the application. Further, the position of the control sensor is as far forward as possible to immediately respond to the thermal demand of the work. The tip and heater are permanently coupled, ensuring that all of the heat generated by the heater is available for use by the tip. For applications where the work cycle is high and for micro-miniature applications the direct power approach is ideal as the thermal demand is continuously monitored and the heater responds immediately by providing adequate power to meet the demand from the work without overshoot.

The SensaTemp® Technology utilises a laser-trimmed platinum RTD sensor that is five times more accurate than a conventional thermocouple. This level of accuracy allows for safe, productive soldering at the lowest possible temperatures. As a result the amount of time spent reflowing each joint is reduced so as to minimise the risk of

damage. The system also allows for tip, heater and handpiece changing without the need for recalibration and acts as a 'thermal reservoir' that minimises tip temperature overshoot, ensures temperature stability and provides reserve power that can be accessed instantaneously for high mass applications.

PACE Worldwide state:

'SensaTemp® delivers consistent, repeatable results regardless of the thermal demand of the work. Its ability to respond quickly is ideal for light work, while its thermal capacity can meet the challenges of the heaviest thermal loads, providing the operator with the flexibility that is essential in today's ever-changing environment.'

The IntelliHeat® Control System allows either SensaTemp® or Tip-Heater Cartridge based technology handpieces to be plugged into a single power source.

Further information is available from PACE Europe Limited, 11 Holdom Avenue, Bletchley, Milton Keynes, Buckinghamshire MK1 1QU. Telephone: 01908 277 666.

SOLUTION FOR LEAD-FREE SOLDER TRANSITION

During the transition from lead containing solders to lead-free solders there is a period in which many soldering operations will require to utilise both lead containing and lead-free solders at the same time. The existence of just one soldering iron or other handpiece on the workbench will ultimately lead to cross-contamination, lower productivity and higher cost.

In order to address this problem PACE Worldwide have developed the ST100, a fully programmable system featuring two IntelliHeat® compatible handpiece channels. This allows for two soldering irons, two mini-tweezers or one of each to co-exist on a workbench.

Contact details as above.

NEW APPROACH TO WIRE-TO-BOARD CONNECTOR DESIGN

A new approach to the design of wire-to-board (WTB) connector design has been developed by ATX.

In place of the traditional contact system and associated insulator is a new arrangement of individual connectors that offer the following benefits:

(i) Replacement of the hard soldering of wires to a PCB, which requires additional labour costs and is not a repeatable manufacturing process.

(ii) Replacement of the two-piece connector systems so as to reduce cost and component count.

(iii) Replacement of the terminal block-style connector so as to allow for mix-and-match contact selection and placement based on AWG, current and voltage specifications, and pick-and-place SMT automated processing.

Three critical design parameters needed to be met in order to achieve a cost-effective contact capable of unprotected performance in harsh environment WTB applications, namely function, size and manufacturability. First and foremost the new contact needed to provide simple, robust and reliable termination of either stranded or solid wires to a PCB. Second, the size of the contact needed to remain minimal so as to enable widespread application. Third, the contact needed to be manufactured economically so that the cost savings realised by the redesign could be passed on to the customer.

In order to be practical the new contact needed to be able to accommodate wire sizes ranging from 12AWG down to 28AWG, and this was achieved by designing three analogous contacts with distinct sizes and mechanical limits. The required electrical performance and mechanical targets for strength of termination were achieved by ensuring that each contact connected with and securely constrained the wire such that the range of AWG for each contact is dictated by the mechanical capabilities of the contact. In order to further expand the functionality of each of the three contacts the wire sizes between contacts are deliberately overlapped as much as possible.

The initial consideration for materials was Beryllium Copper for its superior strength and long-lasting fatigue performance, but a high-performance copper alloy material that was significantly cheaper was eventually selected as it would still exhibit robust performance and long-term reliability.

The closed-box contact design provides a guided, four-sided aperture for the wire to be inserted into and takes up the smallest area possible on the PCB. The top and bottom tines guide the wires into the centre target zone of the right and left contact beams, whilst the lower box section provides a suitable flat area for soldering, ensuring maximum mechanical attachment to the PCB. The top side features a vacuum nozzle pick-up area that allows contacts to be pulled out of the tape and reel packaging during an automated placement process.

The AVX 9296 series of insulator-less contacts is said to have “markedly redefined WTB connectors”.

THE NPL ELECTRONICS INTERCONNECTION GROUP

Over the past two decades the electronics manufacturing industry has successfully faced a series of major challenges ranging from the elimination of CFCs, extensively used for cleaning PCBs, through ever-increasing miniaturisation and the use of new materials and processes, to the implementation of lead-free soldering technologies.

These technological advances have been greatly assisted by the UK funded National Physical Laboratory Electronics Interconnection Group, with industry collaborative

programmes that have not only generated the technology itself, but also have been key to the successful transfer of such technology to the industry.

Currently, issues relating to the reliability of joints, especially those assembled using new lead-free solders, represent an area of major concern for the electronics industry, and in this The NPL Electronics Interconnection Group has been particularly active in defining R and D capabilities, Investigative Studies and Testing. Key areas have included:

- Materials characterisation (e.g. lead-free solders).
- Components stability and evaluation (e.g. termination finish).
- PCB design, assembly and performance (e.g. new processing parameters).
- System performance appraisal (sensitivity to temperature and strain rate).
- Joint lifetime and reliability prediction (suite of computer tools available).
- Materials and components evaluation (e.g. laminate, board finish, solder mask, flux, adhesives, residues).
- Conductive Anodic Filamentation (CAF or whisker growth and effect on board reliability).

As an example of the latter NPL highlight the case of a manufacturer that had experienced problems with the growth of a conductive path from a copper barrel where ionic residues were liable to be trapped. CAF is sensitive to the board material, the design spacing of the through holes, and other factors such as processing temperature and the number of temperature excursions. A matrix study of a number of PCBs that were representative of the manufacturer's current and future products was undertaken by NPL, the results of which successfully defined not only new design rules for producing CAF-free PCB products, but also relevant CAF test regimes.

At National Electronics Week NPL were keen to promote the Group and its associated knowledge base and expertise.

Further information may be obtained from Dr. Chris Hunt on 020 8943 7027. Email: chris.hunt@npl.co.uk

ELECTRONICS COOLING CFD TRENDS: PAST, PRESENT AND FUTURE

In 1989 Computational Fluid Dynamics (CFD) was introduced to the electronics industry by Harvey Rosten and Dr. David Tatchell. They pioneered the move away from general purpose CFD software which could simulate any fluid flow situation into application-specific CFD software that was designed to efficiently solve a single class of problem. This revolutionised electronics cooling by drastically reducing the amount of time necessary to develop sound thermal designs. Instead of iterating

between painstaking hand calculations, prototype building, testing and redesign, engineers could simulate a digital prototype.

The revolution of 1989 led to a drastic reduction in thermal design margins for electronic equipment, but since then there have been comparatively few advances in this area until very recently.

In the paper 'Electronics Cooling CFD Trends: Past, Present and future' Senior Applications Engineer for Future Facilities Inc. explains how intelligent software such as 6SigmaET has led to drastic changes:

"Instead of relying on the engineer to correctly form collections of generic cuboids into the items to be modelled and get the gridding right, 6SigmaET has specific items for specific functions. For example, it knows that a heatsink is a finned, conducting solid that requires airflow for adequate cooling. It knows that fans are controlled by sensors, and it knows that PCBs come with layers, traces and percent copper regardless of the units used.

It is now possible to seamlessly import MCAD and ECAD data into the solution domain while retaining all the relevant details. Gridding is done automatically and intelligently rather than just by keypoint.

Today engineers can model the internal details of a component and analyse it directly in a rack; a concept not even in the minds of thermal engineers ten years ago. Today we understand that it is the power of the component that costs millions of dollars to cool in the data centre, and these costs are now the focus of attention of several large companies such as Facebook, Intel and Hewlett Packard."

A key message from the paper is that thermal engineers no longer have to be specialists:

"By leveraging MCAD and ECAD data and by using intelligent software, most issues can be analysed by a generalist. It does not mean that thermal engineers are no longer necessary, or that anybody can do thermal design. The engineer must still understand the design purpose and cycle. In fact it is streamlining the design process that is necessary in future software development, aiding the engineer, not replacing him or her.

Thermal tools that develop niches in areas that do not look at the design cycle and the role engineers play in that process will not prevail in the market place. MCAD for example is usually done after initial design models have been run. It will never make sense to create detailed MCAD geometry before some basic thermal, mechanical and electric understanding is established."

Copies of the paper are available from Tom Gregory, Consultant Engineer, Future Facilities, 1 Salamanca Street, Albert Embankment, London SE1 7HX. Telephone: 020 7840 9540. www.futurefacilities.com

THERMAL SIMULATION IN THE ENGINEERING DESIGN PROCESS

The paper with the above title by Tom Gregory and Future Facilities Product Manager Dr. Chris Aldham builds on the theory described in the previous paper, this time specifically explaining the practical application of CFD to the engineering design process for electronic equipment. Of particular interest are the advantages of applying thermal simulation at an early stage as well as throughout the design process, and the management of data flow between the thermal engineer and the engineering design team.

The Engineering Design Process

Across the electronics industry the requirement for shorter design and development cycles is increasing. Consequently engineering management has to reduce and manage the risk of design mistakes in every aspect of the product design. In the past detailed thermal design of a product has been a neglected area with 'rules of thumb' used to ensure that components operate at below their maximum operating temperature:

'Mistakes in the thermal design of the equipment would only be found at the prototype stage or even later. Engineers would have to rush to find a solution at a very late stage in the design process. This often resulted in missed deadlines and increased costs.'

The authors argue that this situation is no longer acceptable, and that it is imperative that the thermal design of the equipment must be considered from the very start of the product design cycle.

Concept Simulation

Before the specification of the product is signed off, it may be necessary to create a simple thermal model of the equipment so as to verify that it is possible to cool the equipment within the constraints of the product specification. This is particularly important if the equipment is to be cooled by natural convection, although it can also be important for equipment cooled by forced convection if there is a limit on the number of fans or the fan speed, for example through maximum noise output.

The simulation can be used to determine whether the device can be cooled given the specified power dissipation, form, size, weight and environmental conditions.

Preliminary Design Simulation

If thermal simulation is only performed when the electronic and mechanical design is complete then this makes it very difficult to make any changes to the design, because any change will significantly affect all other aspects of the design. The authors therefore recommend that thermal simulation be performed in tandem with the electronic and mechanical design stages:

'The PCB designer should share key information with the thermal engineers – the components that are expected to be on the board, their approximate location, and an estimate of the power consumption of any significant components'.

This information should enable the thermal engineer to create a thermal simulation, which may in turn identify cooling issues with the board layout. Should the model identify any concerns related to cooling, these can be communicated to the PCB designer before the time consuming task of designing the routes on the board is commenced. Thereafter thermal simulation can be used to experiment with improvements to the PCB design and identify the optimum solution to resolve any cooling issues.

The initial mechanical design that is presented to the thermal engineer need not be a complete 3D model of the enclosure. Simple sketches with key dimensions will suffice to create a simulation that is capable of identifying any major thermal design flaws and regions where there is a risk of a thermal issue.

At this preliminary stage the objective is to identify any areas or components that could potentially have a thermal issue rather than to predict definitive component temperatures or approve the thermal design.

Final Design Simulation

When the design of the equipment is complete a thermal simulation is needed to verify it before any prototypes are produced. This will then ensure that when the equipment is running at maximum load and maximum ambient temperature, all of the components will be below their stated maximum operating temperature. At this point it is necessary to include all thermally relevant information including PCB design, component thermal models, 3D CAD models and material characteristics.

Once the simulation has been created and analysed, a decision can be made as to whether the equipment is ready from a thermal perspective to proceed to manufacture.

Verification

Once a decision has been made to commence prototyping, physical measurements are needed to verify that the thermal simulation is accurate. The accuracy and limitations of the sensors need to be considered:

'There will always be some discrepancy between the simulation and measured results due to experimental accuracy, input data accuracy and numerical accuracy. As long as the discrepancy is not significant, the insight and understanding the simulation gives will still be valid and useful conclusions can be drawn.'

Data Flow

The thermal engineer needs a large amount of data to create an accurate thermal simulation of a piece of electronic equipment. Increasingly thermal design engineers are creating thermal models from a 3D CAD model, and thermal simulation software such as 6SigmaET from Future Facilities is allowing the direct importation of 3D

CAD into the thermal model. The complete 3D model can then be used in the thermal simulation. This enables faster model creation as the thermal engineer no longer has to recreate the geometry in the thermal model.

Sometimes the mechanical engineer may have to simplify the CAD geometry and remove the unnecessary detail, such as the detail on a screw head, before it can be used for the thermal simulation. This reduces the computational complexity of the model and enables the results to be calculated in a reasonable amount of time, without compromising accuracy.

With a direct CAD import into a thermal model, the mechanical engineer should be able to quickly exchange any design changes with the thermal engineer. A procedure is therefore needed such that if any thermally significant change is made to the mechanical design, an updated CAD model can be provided to the thermal engineer.

The authors make the following recommendation:

'Data about the thermal characteristics of all of the material used in the equipment is required for an accurate thermal model. A library of materials and their thermal characteristics should be created and maintained by the thermal engineer. The thermal simulation software should contain a populated library of materials, which can be used across multiple projects. A library can also be used to store fan characteristics of commonly used fans as well as CAD models of parts which are used across multiple projects. Maintaining a comprehensive library will significantly reduce the amount of time that is required to create a thermal model.'

Given the hundreds, or even thousands, of components, the high number of conductor layers, and the thousands of connections on a PCB, creation of a thermal model of a PCB can be challenging, but it is greatly simplified by software such as 6SigmaET and PCB file exchange formats that allow PCB designs to be quickly imported into the model. Detail of the traces on each PCB layer can also be imported and although detailed trace information is often too complicated to solve in a thermal model there are options available to approximate, for example, what percentage of copper trace there is in each area.

In order to accurately predict the component temperature, a thermal model that represents the internal structure of the component is required, and there are two standards for thermal models of electronic components:

(i) The 2-resistor specification (the most commonly supplied information by manufacturers and also the simplest).

(ii) The Delphi-compact model (more detailed and allows for better component temperature prediction).

Thermal engineers need a library of thermal models of components because a thermal model is of little use without accurate information about the power dissipation of the components used in the equipment. The power dissipation needs to be calculated by the electronics engineer who designed the circuit since the power dissipation of a component will vary depending on the application.

The ability to import a list of component power dissipations matched to the component reference designators is key to accelerating future edits to the model as the design evolves.

Component overheat plots show whether the components are operating below the maximum operating temperature. Streamline plots show the airflow through the equipment. The ability to plot the surface temperature directly on imported CAD geometry makes identifying the hot spots in the equipment relatively simple.

This paper is also available from Tom Gregory as above.

CASE STUDY: THALES GLOBAL SERVICES

The Hardware department of Thales Global Services, with a remit traversing all of the Thales divisions, has just carried out thermal simulations of a complex electronic component at an unprecedented level of detail. In modelling the FpBGA, it has been possible to import all the copper tracks, for the component and the board, in an STL format with the aid of the powerful functionality of 6SigmaET.

These tracks did not undergo any simplification and the construction of a detailed model proved to be possible in less than an hour of work time. Such a fine-grained representation of reality has not been achieved before.

The performance of the solver allowed the 125-million grid cell model to run for two days on a PC with eight cores with a clock frequency of 3.05GHz and 48GB of RAM.

Thales Global Services plays an important role as the creative R and D centre for the Hardware Design teams in Thales Group, and provide thermal models for the Corporate Component Database that is used in the design phase of new equipment.

The technological evolution of packages that facilitate 3D design has allowed for increasingly accurate physical representations that include:

- Precise modelling of complex geometrical shapes
- Materials with properties that vary with temperature
- Parts of very different sizes
- Consideration of secondary effects such as Joule Heating.

The creation of a highly detailed model simulating the thermal behaviour and validating the results is a vital step in the process of creating an effective compact model in the form of a Resistor-Capacitor (RC) network which reproduces, with sufficient precision, the transient thermal behaviour of a real component.

For this Thales used the Delphi methodology of imposing multiple boundary conditions on a 3D component, and a genetic algorithm to extract complex RC networks.

The results calculated with 6SigmaET were compared with measurements conducted by US company Analysis Tech, in which the component was mounted on a test board corresponding to the JEDEC standard (100mm x 110mm x 1.6mm). In still air, with the upper face of the board perpendicular to gravity, the thermal resistances Junction/Ambient measured for the two samples were found to be 29.2 degrees Centigrade/W and 30.6 degrees Centigrade/W for a chip power dissipation of 2W. The value obtained by simulation was found to be 30.1 degrees Centigrade/W, and it was therefore concluded that the simulation value was 'in excellent agreement' with the physically measured values.

With this important step in the modelling of electronic components achieved, it was now possible to:

(i) Embark with confidence on the process of compact modelling.

(ii) Verify the design rules of the package, such as the minimal size of the chip.

(iii) Predict the thermal performance of the component in its product environment.

(iv) Identify the thermo-mechanical constraints that could potentially damage the reliability of the package, such as the temperature differences between the BGA balls.

In the future the thermal performance of the BGA 208 package is to be calculated by simulation in the following scenarios:

- Using a JEDEC board without an internal copper plane (2SOP).
- Cooling of the board by forced convection.
- A transient treatment of the board.
- Different orientations of the BGA component.

This paper (by Angelo Greco, Valentin Bissuel and Eric Monier-Vinard of Thales Global Services, Meudon-la-Foret, France) is also available from Tom Gregory.